LATCHING MICRO MAGNETIC RELAY PACKAGES AND METHODS OF PACKAGING

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application Serial Number 60/322,841, entitled MICRO MAGNETIC SWITCH FABRICATION AND APPARATUS, filed 17 September 2001.

Field of the Invention

This invention relates to latching micro magnetic relays.

More particularly, the present invention relates to methods of packaging latching micro magnetic relays and the various packages.

Background of the Invention

Recently, novel latching micro magnetic relays were discovered. The novel latching micro magnetic relay is

based on preferential magnetization of a soft magnetic cantilever in a permanent external magnetic field. Switching between two magnetic states is accomplished by momentarily changing the direction of the cantilever's magnetization by passing a short current pulse through a planar coil situated adjacent the cantilever. Once the relay is switched, it is held in this nonvolatile state (latched) by the permanent external magnetic field. Additional information as to the construction and operation of the novel latching micro magnetic relay is disclosed in a copending United States patent application entitled "Electronically Switching Latching Micro-Magnetic Relay and Method of Operating Same", with serial number 09/496,446, filing date 02 February 2000, and incorporated herein by reference. While a specific latching micro magnetic relay is described above, it will be understood that other Micro Electro Mechanical Systems (MEMS) devices that incorporate magnets are also included in this description.

In the prior art, the cantilever for micro magnetic switches was fabricated as a complete portion of the switch by providing a sacrificial layer of photoresist, depositing the material of the cantilever on the surface of the photoresist and then etching or otherwise dissolving the photoresist layer to provide a cantilever. One problem with

this prior art method is that any process steps performed subsequent to the application of the photoresist layer are seriously limited because of potential damage to the photoresist material and, thus, potential faults or weaknesses in the final product.

Also, in most prior art packaging techniques relatively high temperatures are required for some of the later steps. These high temperatures can seriously affect magnets and some of the other components enclosed in the packages. Further, the materials that could be used as the supporting substrate for the MEMS devices is seriously limited by the fabrication and packaging techniques.

It would be highly advantageous, therefore, to remedy the foregoing and other deficiencies inherent in the prior art.

Accordingly, it is an object the present invention to provide a new and improved latching micro magnetic relay and package.

Another object of the present invention is to provide a new and improved latching micro magnetic relay package that can be fabricated on a variety of substrates.

Another object of the present invention is to provide a new and improved latching micro magnetic relay package that is easy and inexpensive to manufacture.

A further object of the present invention is to provide a new and improved latching micro magnetic relay package fabricated with low temperature assembly.

Still another object of the present invention is to provide a new and improved latching micro magnetic relay package that can be hermetically sealed on any of a variety of improved substrates using relatively low temperature.

Summary of the Invention

Briefly, to achieve the desired objects of the present invention in accordance with a preferred embodiment thereof, provided is a method of forming a package and sealing a MEMS device in the package including the steps of providing a supporting substrate, forming at least one contact for the MEMS device on the surface of the supporting substrate and providing an external connection to the contact, forming a cantilever on the surface of the supporting substrate, the cantilever being positioned to come into electrical engagement with the contact in one orientation, and depositing a seal ring on the surface of the supporting substrate circumferentially around the contact and the cantilever. The method further includes the steps of forming a cap member with a cavity and a continuous edge circumferentially around the cavity, the cavity being designed to receive the cantilever and contact therein, and depositing a seal ring on the continuous edge of the cap member. The package is then sealed by sealingly engaging the seal ring on the continuous edge of the cap member to the seal ring on the surface of the supporting substrate.

In a preferred and more specific embodiment, the sealed package includes a supporting substrate with a surface, at

least one contact for the MEMS device on the surface of the supporting substrate with an external connection to the contact and a cantilever on the surface of the supporting substrate, the cantilever being positioned to come into electrical engagement with the contact in one orientation. A metal seal ring is fixed on the surface of the supporting substrate circumferentially around the contact and the cantilever. A cap member is formed with a cavity and a continuous edge circumferentially around the cavity. The cavity is designed to receive the cantilever and contact therein with the continuous edge in mating engagement with the metal seal ring on the surface of the supporting substrate. A metal seal ring is fixed on the continuous edge of the cap member. The metal seal ring on the continuous edge of the cap member is sealingly engaged with the metal seal ring on the surface of the supporting substrate. In the preferred embodiment the two metal seal rings are sealingly engaged or fixed together by a solder alloy that is reflowed in an inert environment without the use of flux.

Brief Description of the Drawings

The foregoing and further and more specific objects and advantages of the invention will become readily apparent to those skilled in the art from the following detailed description of a preferred embodiment thereof, taken in conjunction with the drawings in which:

FIG. 1 is a simplified sectional view illustrating one embodiment of a wafer scale packaging process for a latching micro magnetic relay;

FIG. 2 is a view in top plan of a pair of wafer as used in the present invention;

FIG. 3 is a simplified sectional view of the wafers of FIG. 2 in alignment, prior to bonding;

FIG. 4 is a more detailed and enlarged sectional view of the wafers of FIG. 2 in alignment, prior to bonding;

FIG. 5 is a more detailed and enlarged sectional view of the wafers of FIG. 4 in alignment, subsequent to bonding;

FIG. 6 is a view in top plan of a portion of the bonded wafers prior to dicing;

FIG. 7 is and enlarged sectional view of a single package after dicing; and

FIG. 8 is a simplified sectional view illustrating portions of another embodiment of a wafer scale packaging process for a latching micro magnetic relay.

Detailed Description of a Preferred Embodiment

Turning now to FIG. 1, a wafer scale package 10 is illustrated for a latching micro magnetic relay or other MEMS structures incorporating a magnet or other heat sensitive components. As will be described in more detail below, one major advantage of package 10 is that it can be assembled using solder preforms and low temperature assembly. Low temperature assembly is desirable because the magnet incorporated in the MEMS structure can easily be damaged by too much heat.

As will become apparent from the discussion below, package 10 can be fabricated in wafer format and does not require the assembly of the MEMS devices individually into individual packages. As described in conjunction with the above structure, a plurality of MEMS devices are generally formed simultaneously on a single wafer. If the wafer must be separated into individual MEMS devices and each individual device packaged separately, the labor cost becomes very high.

In this specific embodiment, a GaAs substrate 12 is used but it should be understood that the substrate could be formed of silicon, glass, quartz, or any other conveneint material that provides the desired characteristics, such as

any of the well known semiconductor material, such as silicon, gallium arsenide, etc., or it can include quartz ceramics, various organic or magnetic materials, etc. Generally, as will be understood by those skilled in the art, a GaAs substrate is preferred because the material provides substantial benefits at higher frequencies. However, the art of silicon processing has developed to a very advanced state in the semiconductor field and is, therefore, very useful in the present invention. Also, in some specific applications, cooperating or externally connected circuitry can be formed directly on the same substrate to reduce connection losses. As will be explained in more detail presently, substrate 12 is generally included as a small portion of a much larger wafer, the individual packages 10 being separated only after substantial portions of the fabrication are completed.

In this preferred embodiment, a pair of vias 14 are provided in substrate 12 and can be formed by any of a variety of well known processes including etching, laser drilling, etc. Generally, the method of formation of vias 14 is determined by the cost of the different procedures. Also, vias 14 are plugged or filled with a conductive material. Technology for plugging or filling vias 14 in GaAs, silicon, or glass exists and will not be elaborated

upon in this disclosure. The lower or external portions of vias 14 are barrier plated for solderability to allow solder bumping or direct solder attachment to a printed wiring board, ceramic board, etc. Also, the lower or external portions of vias 14 form an I/O interface which in the finished format allow for the clearance of the finished package off the surface of a mounting board (not shown).

In general, once vias 14 in substrate 12 are plugged, fabrication of a MEMS device 15 on substrate 12 proceeds in a normal fashion. Because virtually any type of MEMS device can be incorporated into package 10, MEMS device 15 is represented in FIG. 1, simply by a cantilever 16 positioned to provide a contact between spaced apart conductive pads 17 and 18 in an activated state. A hermetic seal ring 20A is positioned around each MEMS device 15 on the wafer (substrate 12). Because a plurality of packages 10 are formed simultaneously on a common wafer, seal rings 20A are all patterned on the wafer surface using common patterning steps.

Seal ring 20A is preferrably metallized onto the surface of wafer 12 and generally includes a thin portion or layer (an adhesion layer) of material or metal that adheres well to wafer 12 (e.g. tungsten, titanium, or combinations

thereof) and a thicker portion or layer (a sealing layer) of a sealing or junction material, e.g., nickel/gold, chrome/gold, etc. Generally, at least a 0.5 mm seal ring 20A around each MEMS device 15 is provided for a hermetic seal. Also, provisions are included for a saw kerf between adjacent die when the wafer is separated into individual packages. A disadvantage is that seal ring 20A and the saw kerf use substantial wafer area, but various procedures and alterations may be incorporated to minimize this problem.

A silicon wafer is provided to form a hermetic cap 22 to be incorporated with a seal ring 20B. While a single cap 22 is illustrated it will be understood that a number of caps will be formed in the silicon wafer equal to the number of MEMS devices formed in the GaAs wafer. Again it will be understood that hermetic cap 22 could be formed from other material, such as glass, ceramic, etc. but silicon is used in this preferred embodiment because of the vast knowledge and machinery available for working with silicon. Anisotropic etching of vias, holes grooves, etc. in silicon wafers is a reasonably well understood process.

A silicon wafer of the right thickness to house a magnet 24 and to clear cantilever 16 of MEMS device 15 is selected. Holes, e.g. circular, square, etc., are etched in

the silicon wafer on a precise pitch. The precise pitch is of course the same pitch used to form MEMS devices 15 and seal rings 20A on the GaAS wafer (substrate 12). Seal ring 20B is metallized on the lower lips of each cap 22 and formed generally as described for seal ring 20A above. To allow a hermetic sealing of cap 22 to substrate 12 an 80/20 Au/Sn preform is tack welded to either metallized seal ring, that is seal ring 20A on substrate 12 or seal ring 20B on cap 22. In another method, 80/20 Au/Sn alloy can be plated on seal ring 20B of cap 22. In this procedure, plating the alloy on the seal ring is believed to be more variable than using a tacked preform.

At any convenient time during the fabrication, a magnet 24 is aligned and bonded (e.g. by epoxy or other suitable adhesive) into the cavity in each cap 22 of the silicon wafer. To this end, using machine vision allows magnets 24 to be precisely placed in the center of each cavity. It will be understood that, in some specific applications, magnet 24 can be placed outside of the package, if desired.

The anisotropically etched caps 22 on the silicon wafer are aligned to the MEMS device on the GaAs wafer and hermetically sealed by reflowing the 80/20 Au/Sn alloy in an inert environment without the use of any flux. Thus, metal

seal ring 20A and metal seal ring 20B are affixed together to form a compound seal ring 20. An appropriate fiducial/alignment scheme can be developed for the wafers to ensure each magnet 24 is aligned to within +/- .001" of the center of each and every MEMS device 15.

The coefficient of thermal expansion of silicon is 2.3 - 4.7 (ppm/C) and for GaAs is 5.4 - 5.72 (ppm/C). There thus would be a minimal mismatch in the coefficient of thermal expansion of about 2 (ppm/C). The consequence of this mismatch is that if stress problems arise in specific application, an Au/Sn alloy which is some what more tin rich could be used to provide the stress relief. In applications where the substrate and cap are formed of similar material thermal expansion is not a problem. The use of other lower temperature solder is possible in all cases as long as fluxless soldering processes are used.

While the above structure provides a complete hermetic seal for the micro magnetic relay or other MEMS structure, it will be understood that in some applications such hermeticity is or may not be required. Thus, in such applications instead of the metal seal rings and/or the solder, the cap may simply be epoxied or otherwise adhered

to the substrate or the seal rings may be epoxied or adhered together.

Finally, a permalloy backing sheet 25 (magnetic flux concentrator) is bonded to the I/O side of the hermetically sealed wafer scale package 10. Permalloy backing sheet 25 is preferrably of a grillage format to allow bonding of all sites (i.e. all packages 10 on the GaAs wafer) at once. The exposed surface of permalloy backing sheet 25 preferrably is provided with an organic dielectric coating. The dielectric coating ensures that no electric paths develop between the external portions of vias 14 or any conductors on the surface of the mounting board. The bonded side of permalloy backing sheet 25 preferrably has a pressure sensitive thermally cureable adhesive thereon. By supplying a pressure sensitive adhesive on permaloy backing sheet 25 assembly can be accomplished very easily.

Generally, an advantage of wafer scale packages 10 is that they can be tested in wafer format (i.e. before separation into individual parts) and then the wafer can be solder bumped if desired. The wafer is then sawn, or otherwise separated, to provide singulated components. Alternatively, the wafer could be sawn to provide singulated components and then tested and individually solder bumped if

desired. Implicit in this procedure is that the wafer die yield is very high (approximately +98%).

Turning now to FIG. 2, a pair of wafers 30 and 32 (device and encapsulation wafers, respectively) are provided. Here it will be understood that wafers 30 and 32 can include any of the well known semiconductor material, such as silicon, gallium arsenide, etc., or they can include quartz ceramics, various organic or magnetic materials, etc. Referring additionally to FIG. 3, it can be seen that an array of latching micro magnetic relays or other MEMS structures are formed on wafer 30 and a similar array of caps are formed in wafer 32. Wafers 30 and 32 are axially aligned in overlying relationship so that a cap in wafer 32 overlies each latching micro magnetic relay or other MEMS structure on wafer 30.

Referring additionally to FIG. 4, an enlarged more detailed sectional view is illustrated of wafers 30 and 32. From this view it can be seen that magnets 34 are positioned in the upper surface of wafer 32 and aligned, one each, with cavities 35 in the lower surface of wafer 32. Wafers 30 and 32 are then brought together and bonded, as illustrated in FIG. 5. Thus, an array of wafer scale packages are manufactured simultaneously in wafers 30 and 32, as

illustrated in FIG. 6. The bonded wafers are then diced, or otherwise separated into a plurality of wafer scale packages. A single one of the wafer scale packages, designated 40, is illustrated in an enlarged sectional view in FIG. 7. The individual packages can be tested before dicing and/or after dicing if desired.

Turning now to FIG. 8, one way to save some of the area required for hermetically sealing wafer scale MEMS package 10 is illustrated. In this procedure, the package is modified from a single plane layout to a multilayer layout. In the multilayer layout of FIG. 8, the structure includes a substrate 50, a permalloy layer 52, a ground plane 54, an insulating dielectric layer 56, and a layer 58 for RF routing and coils. Here it is also assumed the the MEMS cantilever (not shown) is mounted in the same plane as the RF lines. Ground plane 54 is formed of electrically conductive but non-magnetic material (e.g. gold or the like) so as not to reduce the effects of permalloy layer 52. Also, capacitance coupling effects can be mitigated by controlling the thickness of dielectric layer 56.

The structure described above can save wafer space but will include additional mask layers and fabrication steps. A polymer dielectric that can be used in lieu of polyimide

and has RF potential because of its low loss, is Dow Chemical's benzocyclobutene (BCB). This material has been used extensively for high density interconnects in multi chip modules. Another possible high frequency dielectric that can be used is one of the formulations of nitride which is inorganic.

Thus, a new and improved latching micro magnetic relay or MEMS package has been disclosed, which is highly adaptable and easy to manufacture. Also, the improved package and methods of fabrication can incorporate a variety of different supporting substrates. Further, a variety of different caps can be easily fabricated and applied to the substrate using low temperature processes. Because the preferred manufacturing process contemplates the simultaneous fabrication of a plurality of packages on a single wafer, the packages can be tested at various points during the manufacturing process and defective packages can be eliminated before too much time and resources are expended.

Various changes and modifications to the embodiments herein chosen for purposes of illustration will readily occur to those skilled in the art. To the extent that such modifications and variations do not depart from the spirit

of the invention, they are intended to be included within the scope thereof, which is assessed only by a fair interpretation of the following claims.

Having fully described the invention in such clear and concise terms as to enable those skilled in the art to understand and practice the same, the invention claimed is: